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A Survey on Different Domino Logic circuit Design for High-Performance and Leakage-Tolerant

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ABSTRACT: Dynamic logic circuits are preferred for high high speed applications. Wide OR gates are used in Dynamic RAMs, Static RAMs, high speed micro-processors and other high speed circuits. In spite of their high performance, dynamic logic circuit has high noise and extensive leakage which has caused problems for the circuits. To overcome these problems Domino logic circuits are prefer which reduce noise immunity and sub-threshold leakage current in standby for wide OR gates. In this paper we compare different domino logic design topologies for lowering the sub-threshold leakage current in standby mode, increasing the speed and increasing the noise immunity. We compare average power, delay, and unit noise gain (UNG) of different circuit design. The simulation results revealed that High Speed Clock Delay Domino (HSCD) circuit gives the better results in terms of reduction in delay and power consumption as compare to other circuits.

KEYWORDS: Wide domino circuit, sub-threshold leakage current, delay, noise immunity

I. INTRODUCTION

POWER dissipation is an important consideration in the design of CMOS VLSI circuits. High power consumption leads to reduction in the battery life in the case of battery-powered applications and affects reliability, packaging, and cooling costs. The main sources for power dissipation are: 1) capacitive power dissipation due to the charging and discharging of the load capacitance; 2) short-circuit currents due to the existence of a conducting path between the voltage supply and ground for the brief period during which a logic gate makes a transition; and 3) leakage current. The leakage current consists of reverse-bias diode currents and sub-threshold currents. The former is due to the stored charge between the drain and bulk of active transistors while the latter is due to the carrier diffusion between the source and drain of the OFF transistors.

Scaling down of threshold voltage results in exponential increase of the sub-threshold leakage current [5]. The supply voltage and threshold voltage scaling trends for Intel's microprocessor process technologies are discussed in [6]. It can be seen from Fig. 1 that the leakage power is only 0.01% of the active power for 1- m technology, while it is 10% of the active power for 0.1- m technology. There is a fivefold increase in leakage power as the technology process advances to a new generation. Projecting these trends, it can be seen that the leakage power dissipation will equal the active power dissipation within a few generations. Hence, efficient leakage power reduction methods are very critical for the deep-submicron and nanometer circuits.

Wide domino logic refers to domino logic gates with N parallel pull down branches when N is greater then 4; that are used to design circuits in microprocessor critical path. By scaling down the technology the sensitivity of the dynamic node to the noise sources has emerged as a serious design challenge. For improving noise immunity and reducing leakage the keeper transistor is added. However, power dissipation increases and

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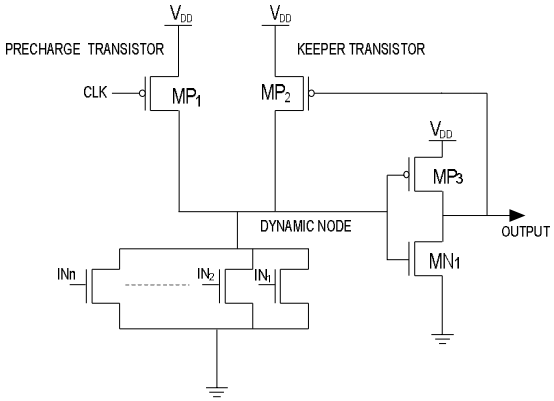

Fig.1 Standard Footerless Domino Logic Circuit

performance degrades by adding this pMOS keeper transistor. Upsizing the keeper transistor improves robustness at a cost of higher power dissipation and delay. The severity increases many fold in wide Domino circuits because of higher number of parallel pull-down branches [2]. Therefore small size keeper is desired for high-speed applications while to increase the robustness, larger keeper is required. Thus, trade off exist between delay and power to improve noise and leakage immunity [3]. Such trade-off is not acceptable because it may increase the delay or make the circuit too power hungry. There are several techniques introduce in the paper to address this issue.

The rest of the paper is arranged as follows. Section II, studies five types of circuits that have been proposed in related literatures, standard footless domino logic, standard footed domino logic, conditional keeper domino logic, high speed domino logic, split domino logic and high speed clock delay domino logic. Simulation results of different methods explained in section II is compare in section III. This comparison includes delay, power, Unit Noise Gain (UNG) for each method and In Section IV we conclude the paper.

II. LITERATURE SURVEY

2.1 Standard Footless Domino Logic Circuit (SFLDL)

The footless scheme [4] is characterized by the fact that discharge of dynamic node is faster. This property is exploited by the high-performance circuits. The circuit of the SFLD logic is shown in Fig1. Operation of Footless-Domino is as follows: During the pre-charge phase, i.e. when then clock (CLK) is LOW, the dynamic node is charged to V_{DD} and the keeper transistor MP_2 turns ON to maintain the voltage of the dynamic node. During the evaluation mode, i.e. when the CLK goes HIGH, the dynamic node is either discharged to ground or remains HIGH depending on the inputs. The size of the keeper transistor should be large enough to compensate for charge sharing problem and at the same time it should be small enough to reduce the contention between the keeper and the nMOS pull down transistor in the case the pull down network evaluates the dynamic node to logic level zero. Otherwise, the pull down network and keeper transistor compete to drive the dynamic node to two opposite directions, this effect is called contention and this results in the degradation of speed.

2.2 Standard Footed Domino Logic Circuit (SFDL)

The footer nMOS transistor MN_2 is connected to the source of evaluation nMOS transistor to obtain the FDL [5] design which basically reduces the leakage current. The speed the SFDL is lower than the footless one because of the stacking effect, but the noise immunity is higher. Fig.2 shows the most conventional footed domino logic circuit. When clock is low, the dynamic node is pre-charged to V_{DD} [7]. In this phase the footed transistor MN_2 is turned off, which reduces the leakage current. When clock goes high, footer transistor MN_2 is turned on. So, depending on incoming data to pull-down network the state of output node is obtained.

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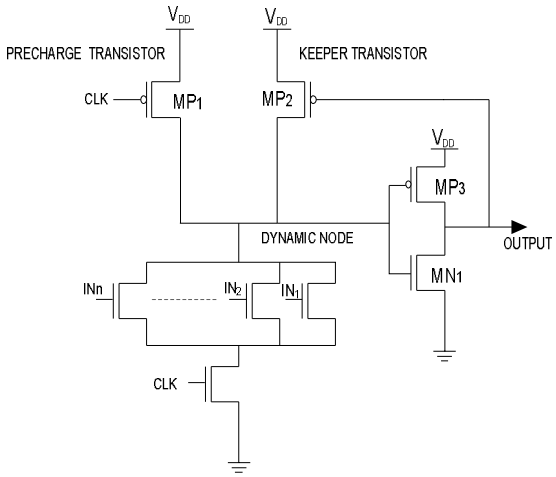

Fig.2 standard footed domino logic circuit

2.3 High Speed Domino Logic (HS)

The circuit of the HS Domino logic is shown in Fig.3 [6]. In HS domino the keeper transistor is driven by a combination of

the output node and a delayed clock. The circuit works as follows: At the start of the evaluation phase, when clock is high, MP_3 turns on and then the keeper transistor MP_2 turns OFF. In this way, the contention between evaluation network and keeper transistor is reduced by turning off the keeper transistor at the beginning of evaluation mode. After the delay equals the delay of two inverters, transistor MP_3 turns off. At this moment, if the dynamic node has been discharged to

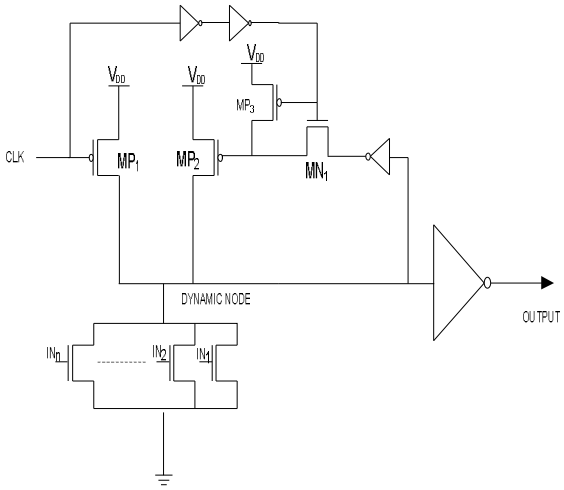

Fig.3 High Speed Domino Logic

ground, i.e. if any input goes high, the nMOS transistor MN_1 remains OFF. Thus the voltage at the gate of the keeper goes to V_{DD}-V_{th} and not V_{DD} causing higher leakage current though the keeper transistor[7]. On the other hand, if the dynamic node remains high during the evaluation phase (all inputs at ‘‘0’’, standby mode), MN_1 turns on and pulls the gate of the keeper transistor. Thus keeper transistor will turn on to keep the dynamic node high, fighting the effects of leakage.

2.4 Conditional Keeper Domino Logic (CKD)

Conditional Keeper employs two keepers, small keeper and large keeper [8]. In this technique, the keeper device (PK) in conventional domino is divided into two smaller ones,PK1 and PK2. The keeper sizes are chosen such that

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PK=PK1+PK2 [9]. Such sizing insures the same level of leakage tolerance as the conventional gate but yet improving the speed.

The circuit works as follows: in pre-charge phase when clock is low, the pull-up transistor is on, so the dynamic node starts being charge up to V_{DD}. At the beginning of evaluation phase when clock is high pre-charge transistors and large keeper PK1 are off. When all the inputs are at low logic level, i.e. in standby mode, the dynamic node after the delays of two inverters remains high, in this condition the output node of NAND gate goes low, this causes the large keeper PK1 to be turned on. The large keeper is deployed after a delay for two inverters, to prevent erroneous discharge of the dynamic node when all inputs remain LOW. The small keeper PK2; however remain ON to compensate for charge leakage until PK1 is activated.

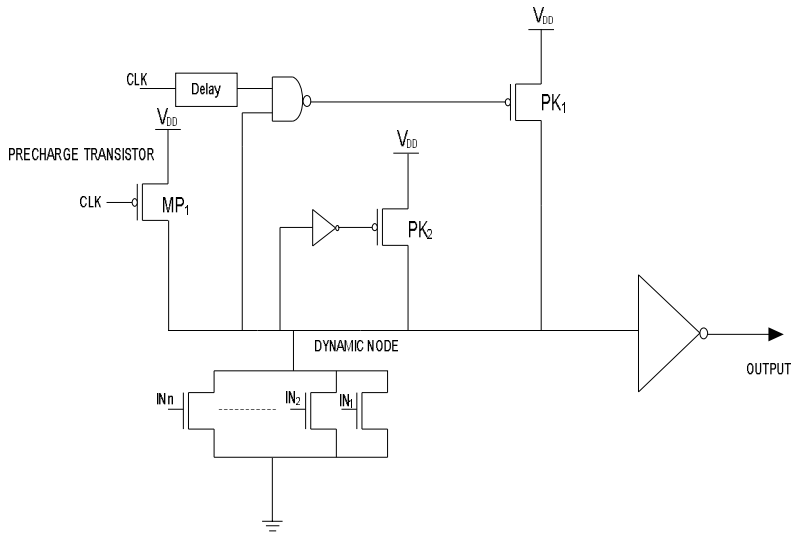

Fig.4 Conditional Keeper Domino Logic

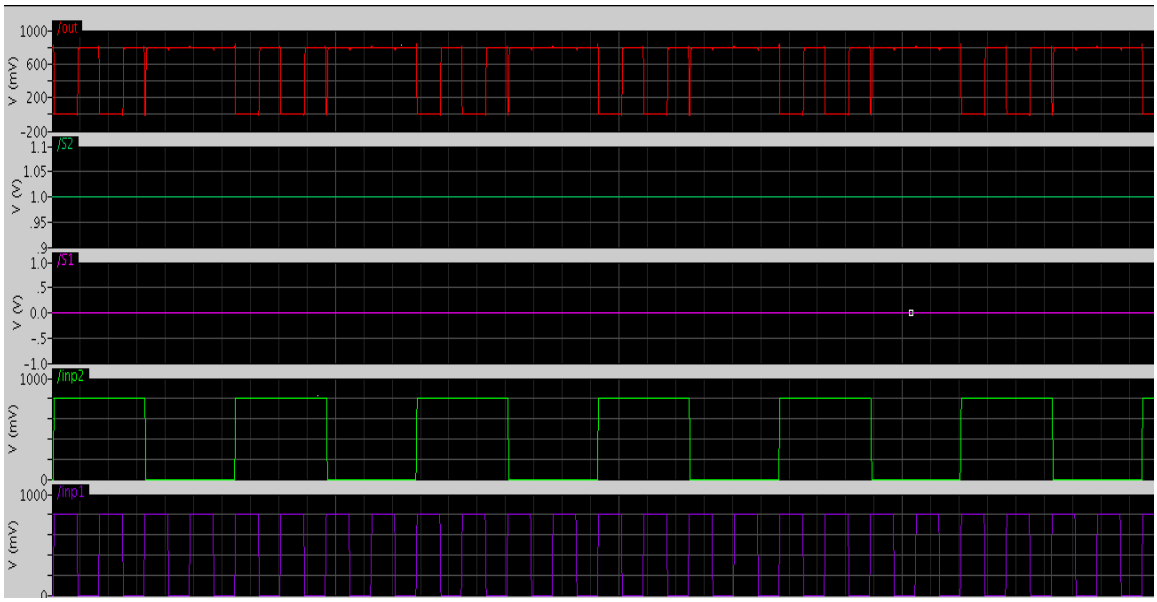

Fig.5. Output wave Form

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2.5 High Speed Clock Delay Domino Logic (HSCD)

Another proposed circuit topology of High Speed Clock Delay Domino circuit[11] is shown in Fig.5. In this circuit footer transistor MN_1 is added to the tail of the evaluation network, which employs stacking effect. Thus the noise immunity improves. At the beginning of the evaluation phase steady state voltage of N-FOOT node is uses to reduce leakage of the evaluation network. The circuit works as follow:

Preacharge Mode: during the preacharge mode when clock is low precharge transistor is turned on which charge the dynamic node to V_{DD}. in addition pMOS keeper transistor is turned on helping the precharge. MN_1 is also ON at the beginning of the evaluation phase which connects the N-FOOT node to ground. Furthermore, node GMN2 is low which is connected to the gate of MN_2 and thus MN_2 is OFF. After the delay equals to the delay of the two inverter (delay element), transistor MN_1 turns off. After the delay of an inverter, MN_1 turns off. In this case, the N-FOOT node voltage rises to an intermediate voltage level. To avoid any possibility of short circuit current in the precharge phase evaluation transistors are sized such that the DC voltage on GMN2 node does not exceed the threshold voltage of MN_2.

Problem Formulation

The main problem in domino logic is that there exist a tradeoff between delay and power. Small size keeper is desired for high-speed applications while to increase the robustness, larger keeper is required. The failure mechanism for a 32-in OR gate using FLDL style at VDD =1V for Temp= 27°C. As it can be seen, due to the large amount of leakage for short channel devices, when a noise pulse is applied to the inputs of the circuit, it fails to operate correctly.

III. Performance Comparison Of Presented Methodes

Simulations are performed in 65 nm technology at 2 GHz frequency and V_{DD} of 1 V. The fall/rise times of the waveforms were set to 1pS. Considering the application of wide OR gates delay, power dissipation and UNG(Unit Noise Gain) has been calculated for 8 input and 16 input OR gate to compare different topologies.
For calculation of UNG [11], a pulse noise is applied to all inputs with amplitude which is a fraction of supply voltage and a pulse width equal to 30% of duty cycle. l. This noise amplitude is defined as

$$UNG= V_{in}, V_{noise} = V_{output}$$

TABLE I
Result for 8 Input OR gate

	Delay	UNG	Power dissipation
SFLD	1	1	1
SFD	1.07	1.01	.85
CKD	1.01	.92	1.02
HS	0.94	1.04	1.11
SD	0.95	0.94	1.21
HSCD	0.93	3.5	1.02

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TABLE II
Result for 16 Input OR gate

	Delay	UNG	Power dissipation
SFLD	1	1	1
SFD	1.09	1.03	0.77
CKD	1.05	0.9	1.05
HS	0.951	0.95	1.13
SD	0.911	0.92	1.24
HSCD	0.907	3.3	1.12

3.1 Application of Domino Logic

Domino logic circuits are basically used to implement wide OR gate. Wide OR gates are used in Dynamic RAMs, Static RAMs, high speed processors and other high speed circuits. Domino logic circuits are thus used which reduce sub threshold leakage current in standby mode and improve noise immunity for wide OR gates

IV. CONCLUSION

In this paper, several domino logic circuit topologies were proposed for high-speed and leakage-tolerant design. High speed clock delayed (HSCD) domino method has the best performance among others. HSCD has a speed improvement of 9% as compared to SFLD and noise immunity also increases. HSCD method can be used for very high speed circuit.

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